REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 01295 to case outlines "E" and "2". Add vendor CAGE 27014 to case outline "2". Change 1.4 (t_{RE}). Convert to military drawing format. Editorial changes throughout. Change Code ident. no. to 67268.	1987 NOV 02	M. A. Frye
B	Add vendor CAGE 18324 for case outlines E, F, and 2. Add case outline F. Changes in electricals on 1.3 and 1.4. Editorial changes throughout.	1988 NOV 28	M. A. Frye

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Marcia B Kelleher

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
08 MAY 1986

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL HCMOS 4-BIT BINARY COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**86076**

SHEET 1 OF 15

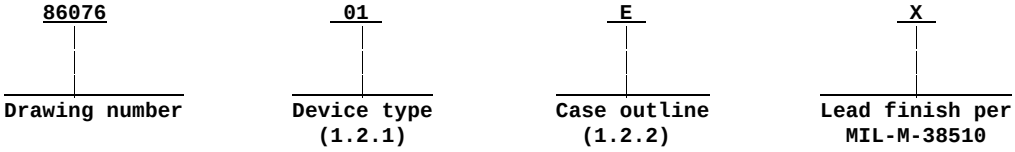
DESC FORM 193-1
SEP 87

5962-E1073

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC163	4-bit synchronous binary counter with synchronous clear

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time	0 to 500 ns

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

Maximum operating frequency (f_{MAX}):	
T_C = +25°C:	
V_{CC} = 2.0 V	**5 MHz**
V_{CC} = 4.5 V	**25 MHz**
V_{CC} = 6.0 V	**29 MHz**
T_C = -55°C and +125°C:	
V_{CC} = 2.0 V	**3.4 MHz**
V_{CC} = 4.5 V	**17 MHz**
V_{CC} = 6.0 V	**20 MHz**
Minimum removal time, reset to clock (t_{re}):	
T_C = +25°C:	
V_{CC} = 2.0 V	**160 ns**
V_{CC} = 4.5 V	**32 ns**
V_{CC} = 6.0 V	**27 ns**
T_C = -55°C and +125°C:	
V_{CC} = 2.0 V	**240 ns**
V_{CC} = 4.5 V	**48 ns**
V_{CC} = 6.0 V	**41 ns**
Minimum setup time, load, or data to clock (t_s):	
T_C = +25°C:	
V_{CC} = 2.0 V	**150 ns**
V_{CC} = 4.5 V	**30 ns**
V_{CC} = 6.0 V	**26 ns**
T_C = -55°C and +125°C:	
V_{CC} = 2.0 V	**225 ns**
V_{CC} = 4.5 V	**45 ns**
V_{CC} = 6.0 V	**38 ns**
Minimum hold time, data from clock (t_h):	
T_C = +25°C:	
V_{CC} = 2.0 V	**50 ns**
V_{CC} = 4.5 V	**10 ns**
V_{CC} = 6.0 V	**9 ns**
T_C = -55°C and +125°C:	
V_{CC} = 2.0 V	**75 ns**
V_{CC} = 4.5 V	**15 ns**
V_{CC} = 6.0 V	**13 ns**
Minimum pulse width clock (t_w):	
T_C = +25°C:	
V_{CC} = 2.0 V	**100 ns**
V_{CC} = 4.5 V	**20 ns**
V_{CC} = 6.0 V	**17 ns**
T_C = -55°C and +125°C:	
V_{CC} = 2.0 V	**150 ns**
V_{CC} = 4.5 V	**30 ns**
V_{CC} = 6.0 V	**26 ns**

Minimum setup time, enable to clock (t_s):
T_C = +25°C:
V_{CC} = 2.0 V - 200 ns
V_{CC} = 4.5 V - 40 ns
V_{CC} = 6.0 V - 34 ns
T_C = -55°C and +125°C:
V_{CC} = 2.0 V - 300 ns
V_{CC} = 4.5 V - 60 ns
V_{CC} = 6.0 V - 51 ns
Minimum hold time, enable, load, or reset to clock (t_h):
T_C = +25°C:
V_{CC} = 2.0 V - 25 ns
V_{CC} = 4.5 V - 5 ns
V_{CC} = 6.0 V - 5 ns
T_C = -55°C and +125°C:
V_{CC} = 2.0 V - 40 ns
V_{CC} = 4.5 V - 8 ns
V_{CC} = 6.0 V - 7 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V			0.4	
High level input voltage 2/	V_{IH}		$V_{CC} = 2.0$ V	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		
Low level input voltage 2/	V_{IL}		$V_{CC} = 2.0$ V	1, 2, 3		0.3	V
			$V_{CC} = 4.5$ V			0.9	
			$V_{CC} = 6.0$ V			1.2	
Input capacitance	C_{IN}	$V_{IN} = 0$ V $T_C = +25°C$ See 4.3.1c		4		10	pF
Quiescent current	I_{CC}	$I_O = 0\ \mu A$ $V_{CC} = 6.0$ V $V_{IN} = V_{CC}$ or GND		1, 2, 3		160	μA
Input leakage current	I_{IN}	$V_{CC} = 6.0$ V $V_{IN} = V_{CC}$ or GND		1, 2, 3		1	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
Functional tests		See 4.3.1d		7			
Propagation delay time, clock to ripple carry output (see figure 4) 3/	t_{PHL1}, t_{PLH1}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			37	
		T_C = -55°C, +125°C C_L = 50 pF μ10%	V_{CC} = 2.0 V	10, 11		340	ns
			V_{CC} = 4.5 V			68	
			V_{CC} = 6.0 V			58	
Propagation delay time, clock to any Q output (see figure 4) 3/	t_{PHL2}, t_{PLH2}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		205	ns
			V_{CC} = 4.5 V			41	
			V_{CC} = 6.0 V			35	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		310	ns
			V_{CC} = 4.5 V			62	
			V_{CC} = 6.0 V			53	
Propagation delay time, enable T to ripple carry output (see figure 4) 3/	t_{PHL3}, t_{PLH3}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		195	ns
			V_{CC} = 4.5 V			39	
			V_{CC} = 6.0 V			33	
		T_C = -55°C, +125°C	V_{CC} = 2.0 V	10, 11		295	ns
		C_L = 50 pF ±10%	V_{CC} = 4.5 V			59	
			V_{CC} = 6.0 V			50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
Transition time (see figure 4) 4/	t_{THL}, t_{TLH}	T_C = +25°C, C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		75	ns
			V_{CC} = 4.5 V			15	
			V_{CC} = 6.0 V			13	
		T_C = -55°C, +125°C	V_{CC} = 2.0 V	10, 11		110	ns
		C_L = 50 pF ±10%	V_{CC} = 4.5 V			22	
			V_{CC} = 6.0 V			19	

1/ For a power supply of 5 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage, so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 60 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.
2/ V_{IH} and V_{IL} tests not required if applied as a forcing function for V_{OH} and V_{OL}.
3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested to the specified parameters.
4/ Transition times, if not tested, shall be guaranteed to the specified limits.

3.2.4 Switching time waveforms. The switching time waveforms shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

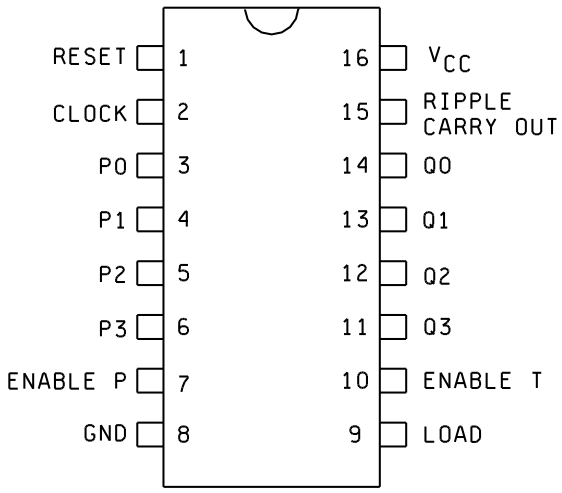
3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

CASE E

PIN ASSIGNMENT



CASE 2

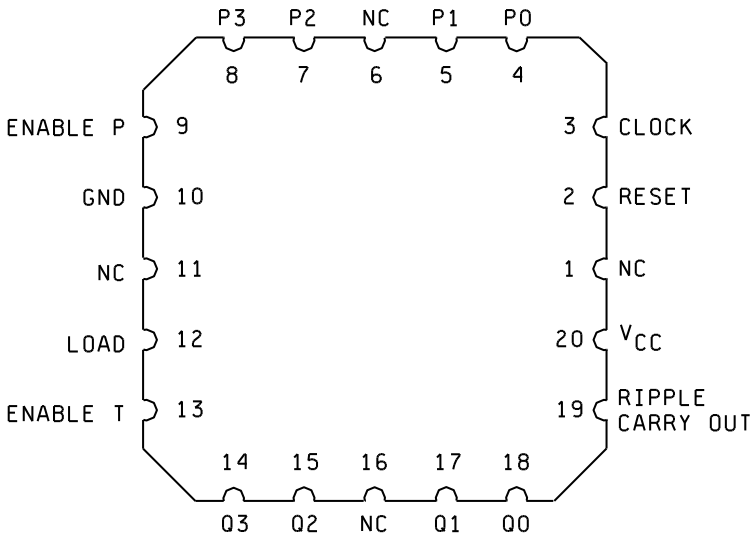


FIGURE 1. **Terminal connections (top view).**

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**86076**
		REVISION LEVEL B	SHEET **8**

Device type 01

Inputs					Outpurs Q
Clock	Reset	Load	Enable P	Enable T	
∫	L	X	X	X	Reset
∫	H	L	X	X	Load preset data
∫	H	H	H	H	Count
∫	H	H	L	X	No count
∫	H	H	X	L	No count

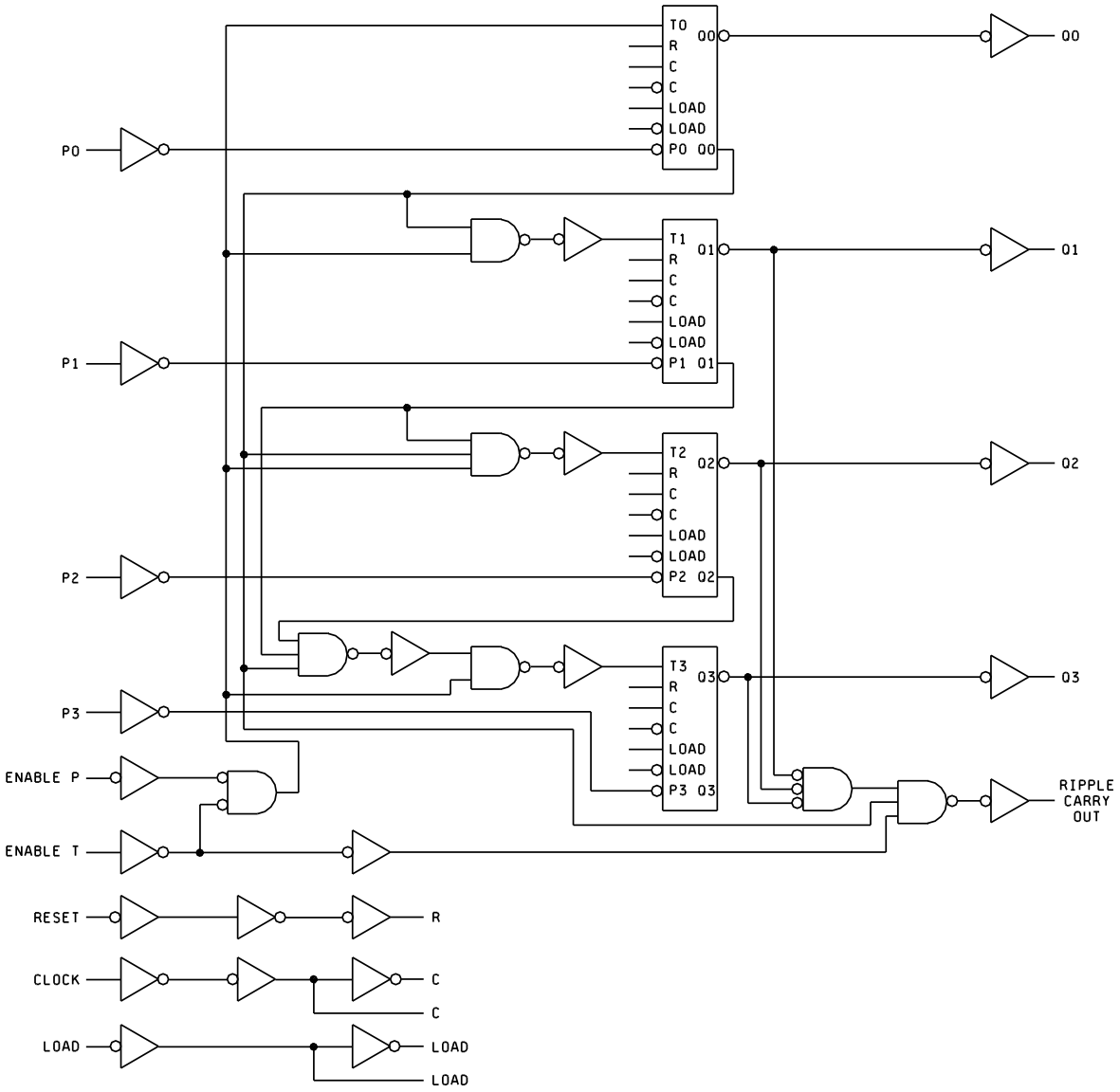
H = high level
L = low level
X = don't care

COUNT/DISABLE

Control inputs			Result at outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple carry out
H	H	H	Count	
L	H	H	No count	High when Q0-Q3 are maximum*
X	L	H	No count	High when Q0-Q3 are maximum*
X	X	L	No count	L

* Q3 Q2 Q1 Q0 = 1111

FIGURE 2. Truth tables.



NOTE:
The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (In) of; the flip-flop. The logic level at the Pn is then clocked to the Q output of the flip-flop on the next rising edge of the clock.
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

FIGURE 3. Logic diagram.

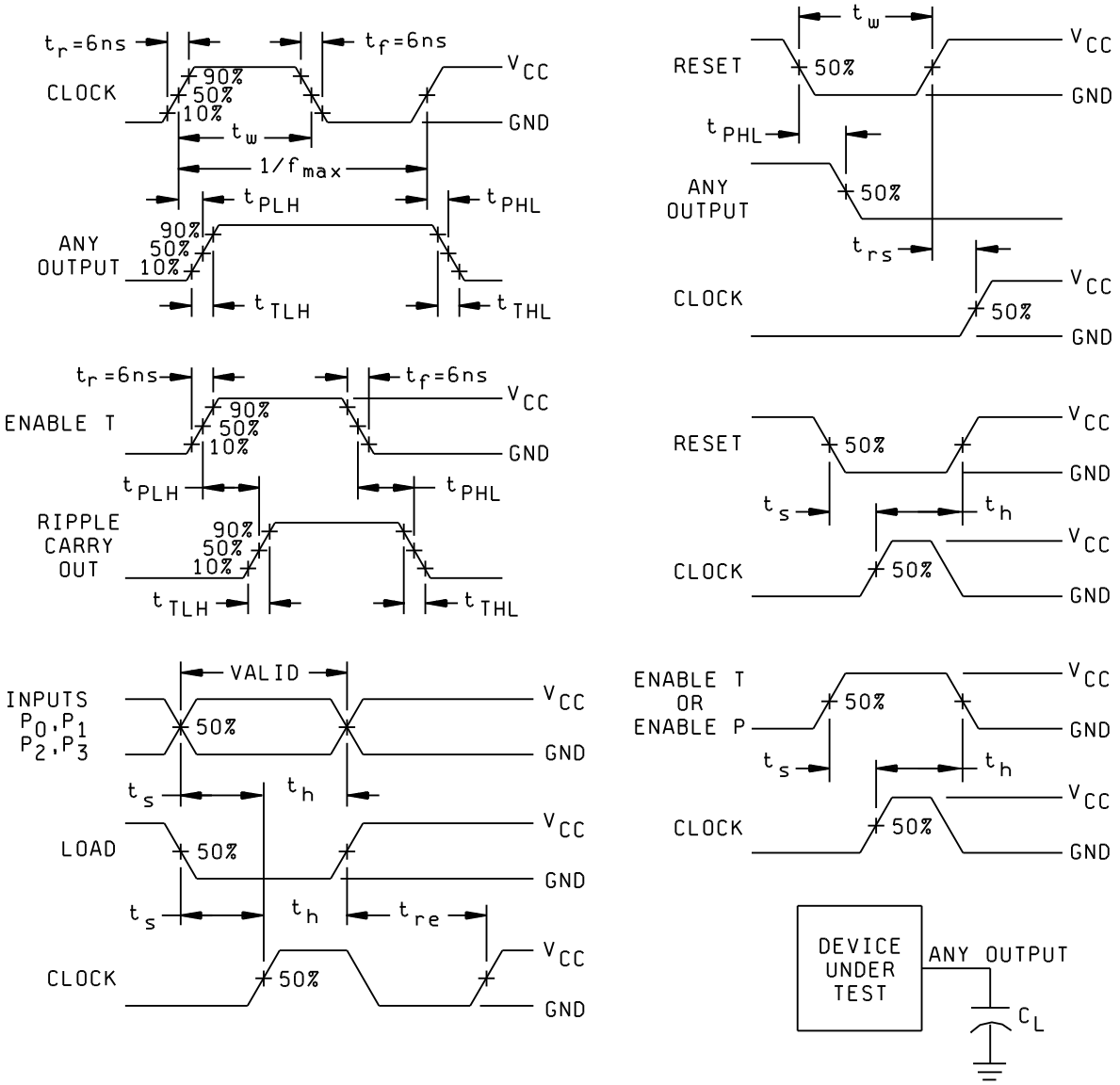
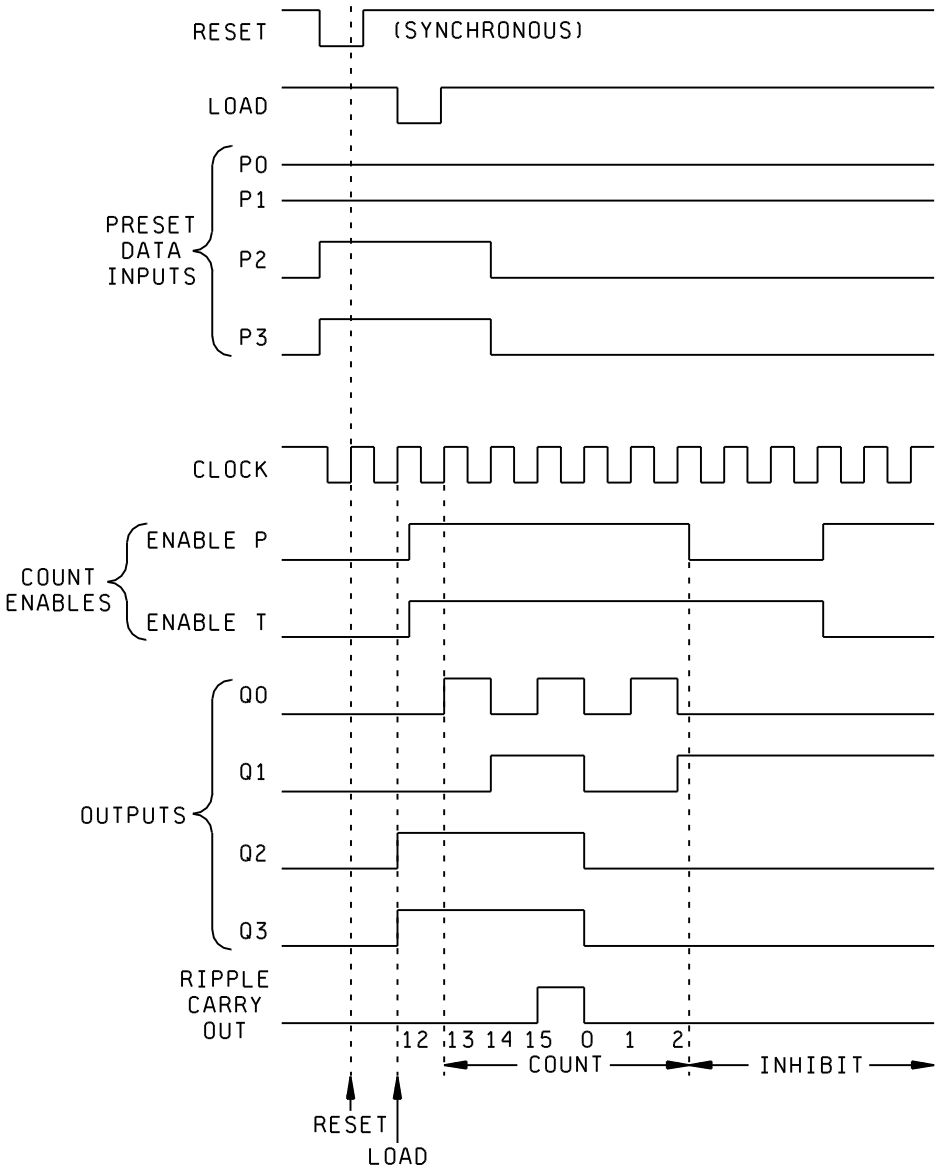


FIGURE 4. Switching time waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**86076**
		REVISION LEVEL B	SHEET **11**



Sequence illustrated in waveforms:
1. **Reset outputs to zero.**
2. **Preset to binary twelve.**
3. **Count to thirteen, fourteen, fifteen, zero, one, and two.**
4. **Inhibit.**

FIGURE 4. Switching time waveforms - Continued.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/66304B--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8607601EX	01295 04713 18714 27014 18324	SNJ54HC163J 54HC163/BEAJC CD54HC163F/3A MM54HC163J/883 54HC163A/BEA	M38510/66304BEX
8607601FX	01295 18324	SNJ54HC163W 54HC163A/BFA	M38510/66304BFX
86076012X	01295 04713 27014 18324	SNJ54HC163FK 545HC163M/B2AJC MM54HC163E/883 54HC163A/B2A	M38510/66304B2X

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated P.O. Box 6448 Midland, TX 79701
04713	Motorola, Incorporated 7402 S. Price Road Tempe, AZ 85283
18714	GE/RCA Corporation Route 202 Somerville, NJ 08876
27014	National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834